

REMARKS

Claims 1-20 are pending in this application. Claims 1-3, 5, 11-13, and 15 have been rejected. Claims 4, 6-10, 14 and 16-20 have been objected to.

The Examiner has objected to the Drawings because the claimed recitation of “ROM” is not shown in the ASIC 215 of the Drawings. In response FIG. 2A has been amended to include a “ROM” component.

The Examiner rejected Claims 1, 2, 11, and 12 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,754,894 (Costello) and Claims 3, 5, 13, and 15 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,400,389 (Niiyama). Claim 1 is now believed to be in allowable condition.

Regarding the Examiner’s rejection of independent Claim 1, Claim 1 has been amended to recite an “interface circuit for copying program data stored in the flash memory according to whether data stored in the flash memory contains errors,” a distinguishing element which is neither disclosed in Costello nor in Niiyama.

Regarding the Examiner’s rejection of independent Claim 11, the Claim has been amended to include the objected to subject matter of dependent Claim 14. Claim 11 is now believed to be in allowable condition.

Claim 14 has been cancelled without prejudice.

Without conceding the patentability per se of dependent Claims 2, 3, 5-10, 12, 13, and 15-20, it is respectfully submitted that they are believed to be allowable by virtue of their dependence on Claims 1 and 11 respectively. Claims 1-3, 5-13 and 15-20 are now believed to be

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Respectfully submitted,



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AMENDMENTS TO THE DRAWINGS

The attached drawing sheet includes a change to FIG. 2A, wherein a previously omitted element, which is described in the specification has been added. Accordingly, please replace the original FIG. 2A with this amended FIG. 2A.

Attachment: Replacement Sheet